11-10-08

for AF

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	Algirdas Avizienis	Before the Board of Patent Appeals and Interferences
Serial No.:	09/886,959	
Filed:	June 20, 2001	
Title:	"SELF-TESTING AND -REPAIRING FAULT-TOLERANCE INFRASTRUCTURE FOR COMPUTER SYSTEMS"	
Our docket:	xAAA-02	Examiner Bryce P. Bonzo Art Unit 2113

PAPER WHICH CORRECTS THE APPEAL BRIEF'S CLAIMS APPENDIX

under 37 CFR § 41.37(c)(1)(viii)

Hon. Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is responsive to the Notice of Non-Compliant Appeal Brief (under 37 CFR 41.37) mailed October 24, 2008.

Attached are:

- a revised Claims Appendix (pages 51 through 74 of the Brief on Appeal); and
- an acknowledgment card for date-stamping and return.

CERTIFICATION OF EXPRESS MAIL DEPOSIT
FOR THE PURPOSE OF SECURING ADVANCED FILING DATE

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Date of Deposit: November 8, 2008

I hereby certify that this document is being deposited with the United States Postal Service as Express Mail under 37 CFR 1.10 on the date indicated above, and is addressed to the Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450.

Signed

Peter P. Lippman

REMARKS and CONCLUSION:

The attached resubmitted Claims Appendix includes pages 59 and 60 with revised claims 37 and 43, to address the inconsistencies asserted in the October 24 Notice at item 7.

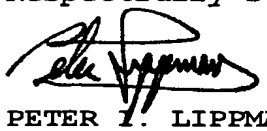
In view of this resubmitted Claims Appendix, Appellant respectfully submits that this case is now ready for docketing as an appeal, and asks that:

- the Brief on Appeal now be accepted as now revised; and
- this case accordingly now be docketed as an appeal; and
- the Board find patentable all of the claims presented on appeal herein, and instruct the Examiner to allow all those claims.

As noted in the Brief, Appellant asks the Board's permission to correct certain minor errors after the appeal is concluded; and — in event the Board disagrees with Appellant as to any of the claims — earnestly asks that the Board provide, under Rule 41.50(c), "an explicit statement of how a claim on appeal may be amended to overcome [any] specific rejection".

Appellant and the undersigned again thank the members of the Board for their patience in considering the many claims and many rejections in this case.

Respectfully submitted,



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November 8, 2008

(10) CLAIMS APPENDIX Pages

Following are all the claims in this case. The one allowed claim, claim 84, is included for the Board's convenience and for completeness.

For the Board's information, the date of most-recent amendment is included for each claim, other than the original claims.

1. (amended May 15, 2006) Apparatus for deterring failure of a computing system; said apparatus comprising:

a hardware network of components, having substantially no software and substantially no firmware except programs held in an unalterable read-only memory;

terminals of the network for connection to such system; and

fabrication-preprogrammed hardware circuits of the network for guarding such system from such failure.

2. (amended May 15, 2006) The apparatus of claim 1, particularly for use with such system that is substantially exclusively made up of commercial, off-the-shelf components; and wherein:

at least one of the network terminals is connected to receive at least one error signal generated by such system in event of incipient such failure of such system;

at least one of the network terminals is connected to provide at least one recovery signal to such system upon receipt of the error signal; and

the apparatus further comprises means for automatically responding to the at least one error signal by generating the at least one recovery signal for guarding all of such system against such failure.

3. (amended October 12, 2005) The apparatus of claim 1, wherein:

the network is an infrastructure which is generic in that it can accommodate any such system that can issue an error message and handle a recovery command.

4. (original) The apparatus of claim 1, further comprising:

such computing system.

5. (original) The apparatus of claim 1, wherein:

the circuits comprise portions for identifying failure of any of the circuits and correcting for the identified failure.

6. (amended October 12, 2005) The apparatus of claim 1, wherein:

the circuits are not capable of running any application program.

7. (amended May 15, 2006) The apparatus of claim 1, particularly for use with a computing system that is substantially exclusively made of commercial, off-the-shelf components and that has at least one hardware subsystem for generating a response of the system to failure; and wherein:

the circuits comprise portions for reacting to such response of such hardware subsystem.

8. (original) The apparatus of claim 1, particularly for use with a computing system that has plural generally parallel computing channels; and wherein:

the circuits comprise portions for comparing computational results from such parallel channels.

9. (amended May 15, 2006) The apparatus of claim 8, wherein:

the parallel channels of such computing system are of diverse design or manufacture.

10. (amended May 15, 2006) The apparatus of claim 1, particularly for use with a computing system that has plural processors; and wherein:

the circuits comprise portions for identifying such failure of any of such processors and correcting for identified such failure.

11. (amended October 12, 2005) The apparatus of claim 1, wherein:

the circuits comprise modules for collecting and responding to data received from at least one of the terminals, said modules comprising:

at least three data-collecting and -responding modules, and

processing sections for conferring among the modules to determine whether any of the modules has failed.

12. (amended May 15, 2006) The apparatus of claim 1, particularly for use with a computing system that is substantially exclusively made of commercial, off-the-shelf components and that has at least one subsystem for generating a response of the system to failure, and that also has at least one subsystem for receiving recovery commands; and wherein:

the circuits comprise portions for interposing analysis and a corrective reaction between such response-generating subsystem and such command-receiving subsystem.

13. (amended May 15, 2006) Apparatus for deterring failure of an entire computing system, wherein the computing system optionally includes plural mutually redundant modules; said apparatus comprising:

a network of components having terminals for connection to such system, wherein the network is constructed to be initially and permanently distinct from such computing system including all of such redundant modules if present; and

circuits of the network for operating programs to guard such entire system from such failure;

the circuits comprising portions for identifying such failure of any of the circuits and correcting for the identified such failure.

14. (amended May 15, 2006) The apparatus of claim 13, wherein:

the program-operating portions comprise a section that corrects for the identified such failure by automatically taking a failed circuit out of operation.

15. (amended October 12, 2005) The apparatus of claim 13, wherein:

the network is an infrastructure that continuously waits to respond to messages from such system.

16. (original) The apparatus of claim 13, further comprising:

such computing system.

17. (amended May 15, 2006) The apparatus of claim 13, wherein:

the program-operating portions comprise at least three of the circuits; and

such failure is identified at least in part by majority vote among the at least three circuits.

18. (amended May 15, 2006) The apparatus of claim 13, wherein:

to guard such entire system from failure, said circuits receive from such system error messages warning of incipient such failure, and issue recovery commands to such system.

19. (amended May 15, 2006) The apparatus of claim 13, particularly for use with a computing system that is substantially exclusively made of commercial, off-the-shelf components and that has at least one hardware subsystem for generating a response of the system to failure; and wherein:

the circuits comprise portions for reacting to such response of such hardware subsystem.

20. (original) The apparatus of claim 13, particularly for use with a computing system that has plural generally parallel computing channels; and wherein:

the circuits comprise portions for comparing computational results from such parallel channels.

21. (amended May 15, 2006) The apparatus of claim 16, wherein:

the computing system has such parallel channels that are of diverse design.

[FOR THE BOARD'S CONVENIENCE: PLEASE SEE CLAIM 70, ADDED MAY 15, 2006 AND PREFERABLY FOR INSERTION HERE.]

22. (amended May 15, 2006) The apparatus of claim 13, particularly for use with a computing system that has plural processors; and wherein:

the circuits comprise portions for identifying such failure of any of such processors, based on error messages from such system, and for correcting for identified such failure.

23. (amended October 12, 2005) The apparatus of claim 13, wherein:

the network is an infrastructure which is generic in that it can accommodate any such system that can issue an error message and handle a recovery command.

24. (amended October 12, 2005) The apparatus of claim 13, particularly for use with a computing system that is substantially exclusively made of commercial, off-the-shelf components and that has at least one subsystem for generating a response of the system to failure, and that also has at least one subsystem for receiving recovery commands; and wherein:

the circuits comprise portions for interposing analysis and a corrective reaction between such response-generating subsystem and such command-receiving subsystem.

25. - 32. (canceled)

33. (amended October 12, 2005) Apparatus for deterring failure of a computing system that is substantially exclusively made of commercial, off-the-shelf components and that has at least one hardware subsystem for generating an error message of the system about incipient failure; said apparatus comprising:

a network of components having terminals for connection to such system; and

circuits of the network for operating programs to guard such system from failure;

the circuits comprising portions for reacting to such error message of such hardware subsystem.

34. (amended October 27, 2005) The apparatus of claim 33, wherein:

in response to such error message, the circuits guard the entire such system from failure.

35. (amended October 12, 2005) The apparatus of claim 33, wherein:

the network is generic in that it can accommodate any such system that can issue an error message and handle a recovery command.

36. (original) The apparatus of claim 33, further comprising:

such computing system, including such hardware subsystem.

37. (amended May 15, 2006) The apparatus of claim 36, wherein:

the computing system has plural generally parallel computing channels; and

such parallel channels of the computing system are of diverse design or manufacture.

38. (amended May 15, 2006) The apparatus of claim 33, wherein:

said circuits are not capable of operating any application program; and are not controlled by any associated host computer that is capable of running any application program.

39. and 40. (canceled)

41. (amended October 12, 2005) The apparatus of claim 33, particularly for use with a computing system that is substantially exclusively made of commercial, off-the-shelf components and that has at least one subsystem for generating a response of the system to failure, and that also has at least one subsystem for receiving recovery commands; and wherein:

the circuits comprise portions for interposing analysis and a corrective reaction between such response-generating subsystem and such command-receiving subsystem.

42. (amended May 15, 2006) Apparatus for deterring failure of an entire computing system that is distinct from the apparatus and that has plural generally parallel computing channels and has at least one application-data input module, and at least one processor for running an application program; said apparatus comprising:

a network of components having terminals for connection to such system; and

circuits of the network for operating programs to guard such entire system from such failure, wherein the network is constructed to be initially and permanently distinct from such computing system including substantially (a) every such application-data input module and (b) every such application-program processor, and (c) all of such parallel computing channels;

the circuits comprising portions for comparing computational results from such parallel channels.

43. (original) The apparatus of claim 47, wherein:

the parallel channels of the computing system are of diverse design.

44. (original) The apparatus of claim 42, wherein:

the comparing portions comprise at least one section for analyzing discrepancies between the results from such parallel channels.

45. (amended October 12, 2005) The apparatus of claim 44, wherein:

the circuits are not capable of running any application program.

46. (amended October 12, 2005) The apparatus of claim 42, wherein:

the network is an infrastructure which is generic in that it can accommodate any such system that can issue an error message and computational results, and handle a recovery command.

47. (original) The apparatus of claim 42, further comprising:

such computing system.

48. (amended May 15, 2006) The apparatus of claim 42, wherein:

the circuits do not and cannot operate any application program; and are not controlled by any associated host computer that is capable of running any application program.

49. (amended May 15, 2006) The apparatus of claim 48, wherein:

to guard such entire system from failure, the circuits receive from such computing system error messages warning of incipient such failure and issue recovery commands to such computing system.

50. (amended May 15, 2006) Apparatus for deterring failure of an entire computing system that is distinct from the apparatus and that has plural generally parallel computing channels; said apparatus comprising:

a network of components having terminals for connection to such system; and

circuits of the network for operating programs to guard such entire system from such failure, wherein such network is constructed to be initially and permanently distinct from such computing system including all of such parallel computing channels;

the circuits comprising portions for comparing computational results from such parallel channels; and wherein:

the comparing portions comprise circuitry for performing an algorithm to validate a match that is inexact; and

the algorithm-performing circuitry employs a degree of inexactness suited to a type of computation under comparison.

51. (amended October 27, 2005) The apparatus of claim 50, wherein:

the algorithm-performing circuitry performs an algorithm that selects a degree of inexactness based on type of computation under comparison; and

the circuits also impose corrective action upon such system based upon discrepancies found by the comparing portions.

[CLAIMS 71 THROUGH 74 WERE ADDED MAY 15, 2006, PREFERABLY FOR INSERTION HERE.]

52. (amended May 15, 2006) The apparatus of claim 42, particularly for use with a computing system that has plural processors; and wherein:

the circuits comprise portions for identifying such failure of any of such processors and correcting for identified such failure.

53. (original) The apparatus of claim 42, wherein:

the circuits comprise modules for collecting and responding to data received from at least one of the terminals, said modules comprising:

at least three data-collecting and -responding modules, and

processing sections for conferring among the modules to determine whether any of the modules has failed.

54. (amended October 12, 2005) The apparatus of claim 42, particularly for use with a computing system that is substantially exclusively made of commercial, off-the-shelf components and that has at least one subsystem for generating a response of the system to failure, and that also has at least one subsystem for receiving recovery commands; and wherein:

the circuits comprise portions for interposing analysis and a corrective reaction between such response-generating subsystem and such command-receiving subsystem.

55. (amended May 15, 2006) Apparatus for deterring failure of any computing system that has plural processors and has at least one application-data input module, and at least one processor for running an application program, and is capable of generating an error message warning of incipient failure and capable of responding to a recovery command; said apparatus comprising:

a network of components having terminals for connection to such system, wherein the network is constructed to be initially and permanently distinct from such any computing system including substantially (a) every such application-data input module and (b) every such application-program processor, and (c) all of such plural processors; and

circuits of the network for operating programs to guard any such system from such failure;

the circuits comprising portions for identifying such failure of any of such processors and correcting for identified such failure.

[CLAIM 75 WAS ADDED MAY 15, 2006,
PREFERABLY FOR INSERTION HERE.]

56. (amended May 15, 2006) The apparatus of claim 75, wherein:

the identifying portions comprise a section that corrects for the identified such failure by taking a failed processor out of operation.

57. (amended October 12, 2005) The apparatus of claim 75, wherein:

the circuits cannot and do not run an application program.

58. (amended October 12, 2005) The apparatus of claim 75, wherein:

the circuits protect the entire such computing system.

59. (amended October 12, 2005) The apparatus of claim 75, further comprising:

such computing system.

60. (canceled)

61. (amended October 12, 2005) The apparatus of claim 75, particularly for use with a computing system that is substantially exclusively made of commercial, off-the-shelf components and that has at least one subsystem for generating a response of the system to failure, and that also has at least one subsystem for receiving recovery commands; and wherein:

the circuits comprise portions for interposing analysis and a corrective reaction between such response-generating subsystem and such command-receiving subsystem.

62. (amended May 15, 2006) Apparatus for deterring failure of an entire computing system that is distinct from the apparatus and has at least one application-data input module, and at least one processor for running an application program; said apparatus comprising:

a network of components having terminals for connection to such system; and

circuits of the network for operating programs to guard such entire system from such failure;

the circuits comprising modules for collecting and responding to data received from at least one of the terminals, said modules comprising:

at least three data-collecting and -responding modules, and

processing sections for conferring among the modules to determine whether any of the modules has failed;

wherein the network, including all of the modules and substantially (a) every such application-data input module and (b) every such application-program processor, and (c) all of the processing sections, is constructed to be initially and permanently distinct from such computing system.

63. (original) The apparatus of claim 62, further comprising:

such computing system.

64. (amended October 12, 2005) The apparatus of claim 62, particularly for use with a computing system that is substantially exclusively made of commercial, off-the-shelf components and that has at least one subsystem for generating a response of the system to failure, and that also has at least one subsystem for receiving recovery commands; and wherein:

the circuits comprise portions for interposing analysis and a corrective reaction between such response-generating subsystem and such command-receiving subsystem.

[CLAIMS 76 THROUGH 78 WERE ADDED MAY 15, 2006, PREFERABLY FOR INSERTION HERE.]

65. (amended May 15, 2006) Apparatus for deterring failure of a computing system that is substantially exclusively made of commercial, off-the-shelf components and that has at least one subsystem for generating a response of the system to failure, and that also has at least one subsystem for receiving recovery commands; said apparatus comprising:

a network of components having terminals for connection to such system between the response-generating subsystem and the recovery-command-receiving subsystem; and

circuits of the network for operating programs to guard such system from such failure;

the circuits comprising portions for interposing analysis and a corrective reaction between the response-generating subsystem and the command-receiving subsystem.

66. (amended August 9, 2004) The apparatus of claim 65, further comprising:

such computing system.

67. (added October 12, 2005) The apparatus of claim 65, wherein:

the circuits cannot and do not run any application program.

68. (amended May 15, 2006) The apparatus of claim 65, wherein:

by responding to an error signal from such system, the circuits protect the entire such system from failure.

69. (added October 12, 2005) The apparatus of claim 65, wherein:

the network is an infrastructure which is generic in that it can accommodate any such system that can issue an error message and handle a recovery command.

70. (amended May 15, 2006) The apparatus of claim 13, wherein:

the circuits do not and cannot operate any application program; and are not controlled by any associated host computer that is capable of running any application program.

71. (added October 12, 2005) The apparatus of claim 50, wherein:

the circuits cannot and do not run any application program.

72. (canceled)

73. (amended May 15, 2006) The apparatus of claim 50, wherein:

to guard such entire system from failure, the circuits receive from such computing system error messages warning of incipient failure and issue recovery commands to such computing system.

74. (added October 12, 2005) The apparatus of claim 50, wherein:

the network is an infrastructure which is generic in that it can accommodate any such system that can issue an error message and computational results, and can handle a recovery command.

75. (added October 12, 2005) The apparatus of claim 55, wherein:

the program-operating circuits guard any such system from failure by issuing a recovery command; and

the failure-identifying and correcting portions provide the recovery command.

76. (added October 12, 2005) The apparatus of claim 62, wherein:

the circuits cannot and do not run any application program.

77. (amended May 15, 2006) The apparatus of claim 62, wherein:

to guard the entire such system from failure, the circuits receive from such computing system error messages warning of incipient failure.

78. (added October 12, 2005) The apparatus of claim 62, wherein:

the network is an infrastructure which is generic in that it can accommodate any such system that can issue an error message and handle a recovery command.

79. (added October 27, 2005) The apparatus of claim 1, wherein:

the apparatus is not a circuit breaker.

80. (amended May 15, 2006) The apparatus of claim 1, wherein:

at least one of the network terminals is connected to receive at least one error signal generated by such system in event of incipient such failure of such system;

at least one of the network terminals is connected to provide at least one recovery signal to such system upon receipt of the error signal.

81. (amended May 15, 2006) An infrastructure for a computing system that has at least one computing node ("C-node") for running at least one application program; said infrastructure being for guarding the system against failure, and comprising:

at least one monitoring node ("M-node") for monitoring the condition of the at least one C-node by waiting for an error signal, indicating incipient such failure, from the at least one C-node and responding to the error signal by sending a recovery command to the at least one C-node; and

at least one adapter node ("A-node") for transmitting the error signal and recovery command between the at least one C-node and at least one M-node; and wherein:

the at least one M-node is manufactured, and remains, wholly distinct from the at least one C-node; and

the at least one M-node cannot, and does not, run any application program.

82. (added October 27, 2005) The infrastructure of claim 81, further comprising:

such computing system.

83. (added October 27, 2005) The infrastructure of claim 81, particularly for use with such computing system that has plural such C-nodes; and further comprising:

a decision-making node ("D-node") for comparing output data generated by such plural C-nodes and reporting to the at least one M-node any discrepancy between the output data; and wherein:

the at least one M-node analyzes the D-node reporting, and based thereon arbitrates among the C-nodes.

84. (allowed August 24, 2006) An infrastructure for a computing system that has at least one computing node ("C-node") for running at least one application program; said infrastructure being for guarding the system against failure, and comprising:

at least one monitoring node ("M-node") for monitoring the condition of the at least one C-node by waiting for an error signal, indicating incipient such failure, from the at least one C-node and responding to the error signal by sending a recovery command to the at least one C-node;

at least one adapter node ("A-node") for transmitting the error signal and recovery command between the at least one C-node and at least one M-node; and wherein:

the at least one M-node is manufactured, and remains, wholly distinct from the at least one C-node, and

the at least one M-node cannot, and does not, run any application program; and

at least one self-checking node for startup, shutdown and survival ("S3-node"), specifically for executing power-on and power-off sequences for such system and for the infrastructure, and for receiving error signals and sending recovery commands to the at least one M-node.